REMARKS

The Applicants respectfully request reconsideration and allowance of claims 1-18 in view of the above amendments and the following arguments.

I. INTERVIEW SUMMARY

The Applicants appreciate the telephone interview conducted on April 3, 2006, between Examiner Tat and Applicants' attorney, Trevor Lind. In the interview, the Applicants' attorney pointed out the differences between the limitations required by independent claims 1, 8, and 13 and the circuit design method disclosed in "Dynamic Logic Synthesis," IEEE, 1997, to Yee et al. ("Yee" or the "Yee article"). No agreement was reached as to the allowability of the claims.

II. AMENDMENTS TO THE CLAIMS

Independent claims 1, 8, and 13 have been amended to require that the logic synthesis block comprises a single dynamic logic circuit. Support for this amendment can be found in the specification of the present application from page 7, line 6 to page 12, line 8 and page 14, lines 15-18.

No new matter has been added by the amendments to the claims. Claims 1 through 18 remain pending in the case.

III. AMENDMENTS TO THE SPECIFICATION

The specification has been amended to correct typographical errors.

IV. CLAIMS 1-18 REQUIRE LIMITATIONS THAT ARE NOT DISCLOSED IN THE YEE ARTICLE

The current Office Action rejects claims 1 through 18 under 35 U.S.C. §102(b) as being anticipated by the Yee article. The Applicants submit that Yee does not anticipate these claims because Yee does not disclose all of the limitations required by claims 1-18.

The present application includes three independent claims, claims 1, 8, and 13. Due to the nature of the claims, claim 8 will be addressed first in the comments below.

Independent Claim 8

Independent claim 8 is directed to a method of synthesizing a logic circuit to provide a predetermined logical operation and requires the following limitations:

(a) defining a logic synthesis block comprising **a single dynamic logic circuit**; and
(b) performing logic synthesis for the predetermined logical operation to produce an intermediate circuit, the logic synthesis utilizing a synthesis library constrained to **the single dynamic logic circuit** comprising the logic synthesis block.

A specific example of a circuit design method implementing the limitations required by claim 8 can be found starting on page 7, line 6 of the specification of the present application. This example defines the logic synthesis block as a four high and four wide dynamic AND/OR circuit ("4A4O"). (See p. 7, line 9 - p. 8, line 13). An intermediate circuit is produced by the logic synthesis tool using the 4A4O circuit in the synthesis library. (See Figure 4 and p. 8, line 14 - p. 9, line 7). The intermediate circuit includes the number of 4A4O circuits needed to implement the predetermined logical function. (See Figure 5 and p. 11, line 17 - p. 12, line 8). The intermediate circuit does not include any other circuit besides 4A4O circuits because the synthesis library utilized during logic synthesis was constrained to using only a single dynamic logic circuit, the 4A4O circuit. Thus, as can be seen from not only the plain language of the claim, but also from the above example, the logic synthesis block of claim 8 comprises simply a

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single dynamic logic circuit, such as a 4A4O circuit, and the logic synthesis required at element (b) of claim 8 is performed using just this single dynamic logic circuit in the synthesis library.

The Yee article discloses logic synthesis using a logic circuit library comprising clock-delayed ("CD") domino circuits. However, Yee does not disclose defining a logic synthesis block comprising a single dynamic logic circuit nor does Yee disclose constraining a synthesis library to a single dynamic logic circuit as required by claim 8. In particular, Yee does not disclose these limitations of claim 8 because the logic circuit library in Yee is made up of a specific family of dynamic logic circuits, that is, a synthesis library of multiple CD domino circuits, as opposed to being made up of only **a single dynamic logic circuit**.

Because the Yee article does not disclose all of the limitations required by claim 8, the Applicants submit that claim 8 is not anticipated by Yee. Claim 8 should therefore be in condition for allowance along with its respective dependent claims, claims 9-12.

Independent Claim 1

Independent claim 1 requires limitations similar to those required by claim 8. In particular, claim 1 requires defining a logic synthesis block comprising **a single dynamic logic circuit** and performing logic synthesis utilizing a synthesis library **constrained to this logic synthesis block**. Thus, the arguments presented above with respect to claim 8 apply with equal force to claim 1. In addition, claim 1 requires eliminating unused devices in the intermediate circuit to produce a final circuit. However, Yee does not disclose any unused devices after logic synthesis takes place nor does Yee disclose the removal of unused devices from an intermediate circuit. Therefore, since Yee does not disclose all of the limitations required by claim 1, the Applicants submit that Yee does not anticipate claim 1.

For these reasons, the Applicants submit that claim 1 is not anticipated by the Yee article and is entitled to allowance along with its respective dependent claims, claims 2-7.

Independent Claim 13

Claim 13 is directed to a circuit design method utilizing a logic synthesis tool and predefined logic circuit library to provide a logic implementation for a predetermined logical operation. The improvements required by claim 13 include defining a logic synthesis block comprising **a single dynamic logic circuit** and **constraining the logic synthesis tool to the logic synthesis block**. As discussed above with respect to claims 1 and 8, the Yee article does not disclose these limitations. Therefore, since Yee does not disclose all of the limitations required by claim 13, the Applicants submit that Yee cannot anticipate claim 13.

For these reasons, claim 13 is entitled to allowance along with its respective dependent claims, claims 14-18.

Dependent Claims 2, 9, and 15

The Yee article also fails to disclose many of the elements required by claims depending from independent claims 1, 8, and 13. For example, dependent claims 2, 9, and 15 require that the step of defining the logic synthesis block includes selecting the largest practical dynamic AND/OR circuit for the integrated circuit fabrication technology in which the circuit is to be implemented.

Item 5 on page 3 of the Office Action cites Figure 8 and page 347 of Yee as showing the limitations required by claims 2, 9, and 15. However, Figure 8 only shows a CMOS OR4 gate and a dynamic OR4 gate. Neither of the gates in Figure 8 is an AND/OR circuit as required by claims 2, 9, and 15. In addition, the second paragraph of Section V on page 347 of Yee states, "Since CD domino provides fast and robust OR, NOR, and NOT gates, AND and NAND gates

were not used in the CD domino benchmarks." Thus, page 347 of Yee indicates that an AND/OR circuit was not used at all in the logic synthesis used to produce the CD domino benchmark circuits analyzed in the Yee article. Therefore, the sections of Yee cited in the Office Action rejecting claims 2, 9, and 15 do not disclose the limitations required by these claims. Furthermore, there is no other disclosure in Yee that shows the limitations required by claims 2, 9, and 15. Since the Yee article does not disclose the limitations required claims 2, 9, and 15, this reference cannot anticipate these claims.

For these reasons, the Applicants submit that claims 2, 9, and 15 are allowable both as being dependent upon an allowable base claim and for the additional limitations that they directly add.

V. CONCLUSION